NOVEMBER 1969

AWM1269

FOUR-BIT MEMORY Serial in, serial out

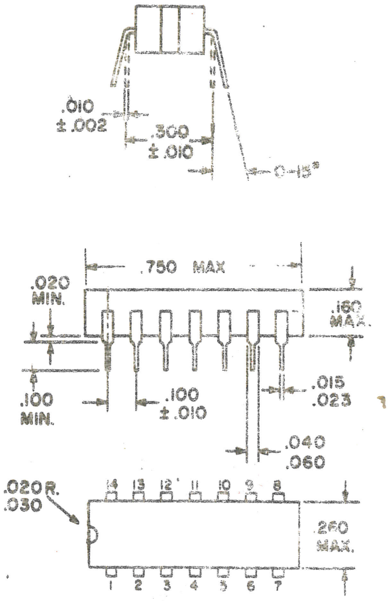
DESCRIPTION

The AWM 1269 is a DTL MSI functional block incorporating a 4-bit store. Data from a common input line is written into a location by applying a logic zero to the corresponding write clock line. Data entry is edge triggered on the negative-going transition of the clock. Data read-out is gated onto a common output line and read-out is enabled by applying a logic zero to the corresponding read clock. Output collectors are "open" to provide for wired-OR coupling to similar units. Simultaneous read and write operations are permitted at different locations.

GENERAL CHARACTERISTICS

Package:	14 pin hermetic Dual-in-line ceramic
Max. storage temp:	140°C
Operating temp. range:	0°C to 70°C
Supply voltage range:	4.5 to 5.5V
Max. input to any pin:	+5.5V
Min. input to any pin:	- 0.5V
Logic Levels:	Compatible with TTL/DTL
Fan out (per line):	2 standard loads
Write cycle time:	45ns (typical)
Power dissipation:	150mW

DIMENSIONAL OUTLINE



(Dimensions in inches)

PIN CONNECTIONS

1. Ground
2. Data out
3. Read Cell 4
4. Read Cell 3
5. Read Cell 2
6. Read Cell 1
7. V_{CC}
8. Ground
9. Data in
10. Write Cell 1
11. Write Cell 2
12. Write Cell 3
13. Write Cell 4
14. Data in

Pins (1,8) (9,14) are internally connected

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INTEGRATED CIRCUIT

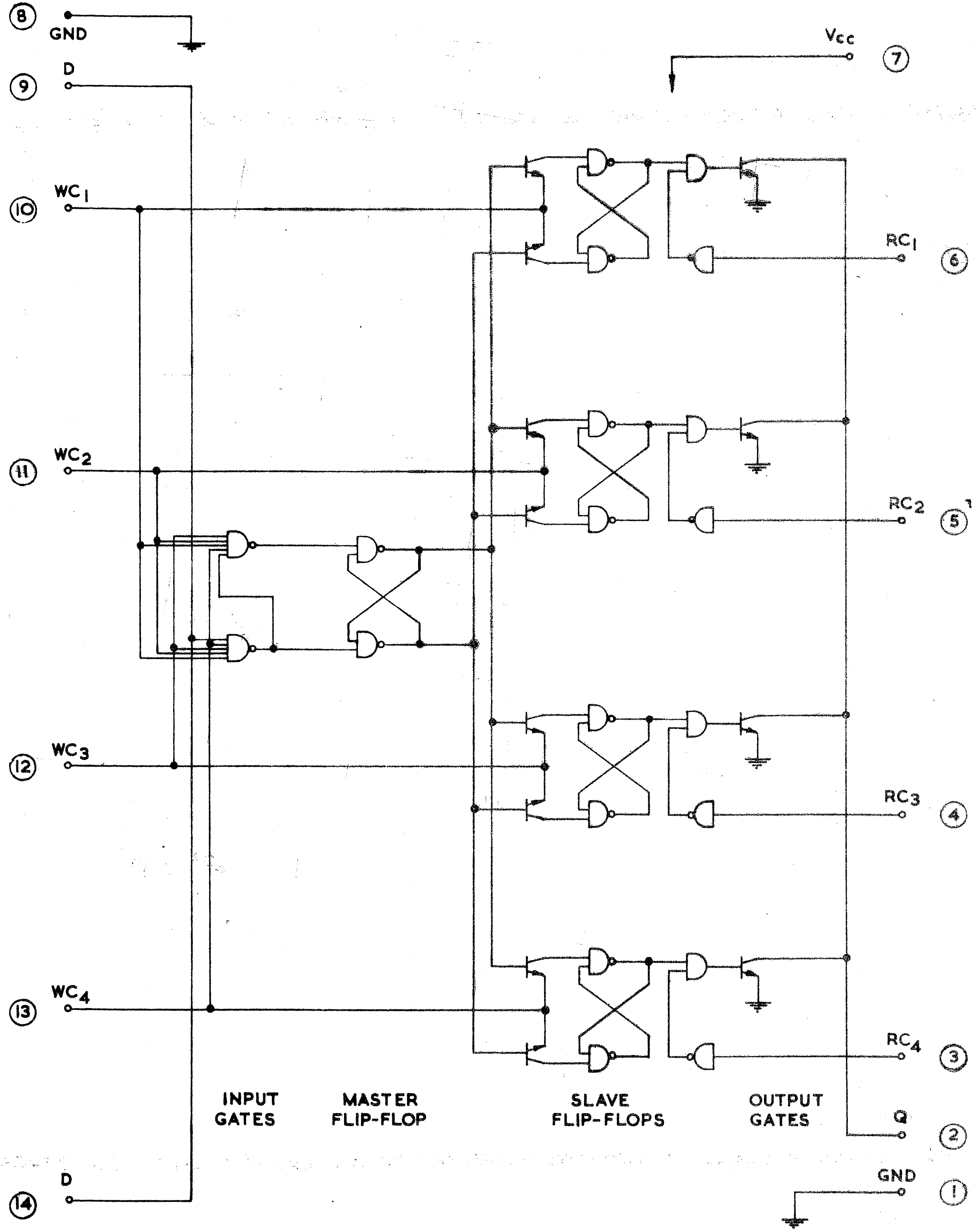


FIGURE 1 FUNCTIONAL SCHEMATIC

PIN	FUNCTION	PARAMETER ($T = 25^{\circ}C$)	FORCING FUNCTION	LIMITS			UNITS
				MIN	TYP	MAX	
1	Ground (Common with 8)						
2	Data out[2] (Q)	High state: current	$V_{OH} = 5V$	0		0.05	mA
		Low state: voltage(V_{OL})	$I_L = 4.8mA$	.25	.35	0.4	V
3	Read clock (RC_4) Cell 4	Read inhibit: voltage(V_{IH})		1.4		5.5	V
		current(I_{IH})	$V_{IH} = 5.0$	0		0.01	mA
		Read enable: voltage(V_{IL})		-.5		0.8	V
		current(I_{IL})	$V_{IL} = 0V$	-1.0	-1.5	-1.8	mA
4	Read clock (RC_3) Cell 3	See (3)					
5	Read clock(RC_2) Cell 2	See (3)					
6	Read clock(RC_1) Cell 1	See (3)					
7	Positive supply	Voltage		4.5		5.5	V
		Current		18	25	35	mA
8	Ground (Common with 1)						
9	Data in (D) (Common with 14)	High state: voltage (V_{IH})		2.0		5.5	V
		current(I_{IH})	$V_{IH} = 5.0V$	0		0.05	mA
		Low state: voltage (V_{IL})		-.5		1.4	V
		current (I_{IL})	$V_{IL} = 0V$	0.5	0.8	1.0	mA
10	Write clock[3] (WC_1) Cell 1	High state: voltage(V_{IH})		2.0		5.5	V
		current	$V_{IH} = 5.0V$	0.02		0.1	mA
		Low state: voltage		0.0		0.9	V
		current	$V_{IL} = 0V$	-2	-3	-4	mA
11	Write clock(WC_2) Cell 2	See (10)					
12	Write clock(WC_3) Cell 3	See (10)					
13	Write clock(WC_4) Cell 4	See (10)					
14	Data in (Common with 9)						

Notes. 1. It is recommended that common pins be externally connected.
2. Output data (Q) is noninverted with respect to D. Output collectors are "open" and an external pull-up resistor should be used to define the high state logic level.
3. On the negative-going clock edge, input data is locked in the master flip-flop for V_I less than 1.4V and transferred to the slave (store) flip flops for V_I less than 0.9V

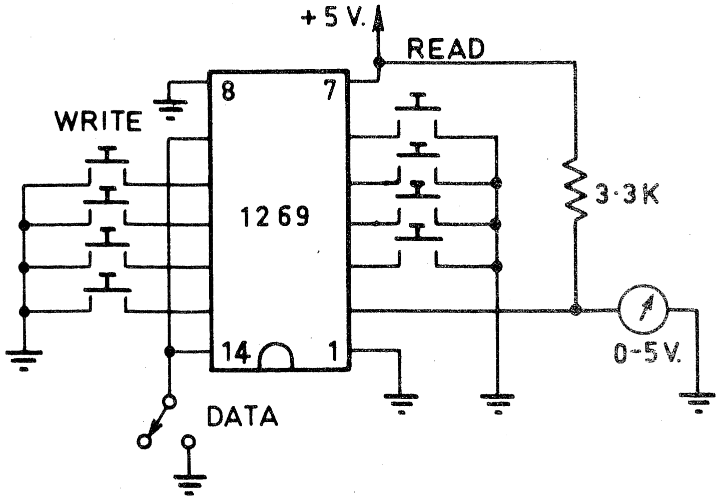


FIG. 2. FUNCTIONAL TEST SET UP.

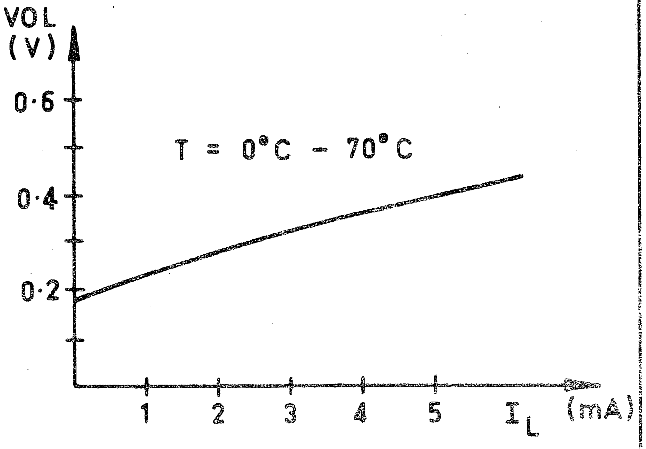
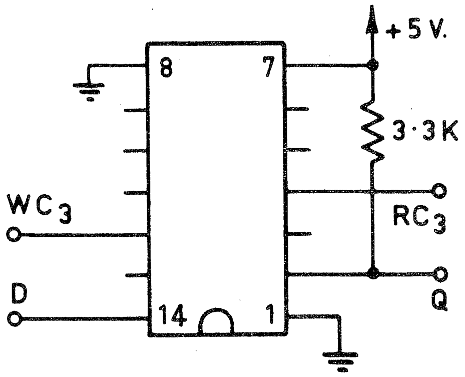


FIG. 3. OUTPUT LOADING CURVE (LOW STATE)



TYPICAL SWITCHING PARAMETERS		
MIN. NEGATIVE CLOCK DURATION	t_c	40 ns
DATA SET UP TIME	t_{ds}	35 ns
DATA HOLD TIME	t_h	15 ns
DATA READ DELAY	t_{p-}	33 ns
	t_{p+}	30 ns

WAVEFORMS

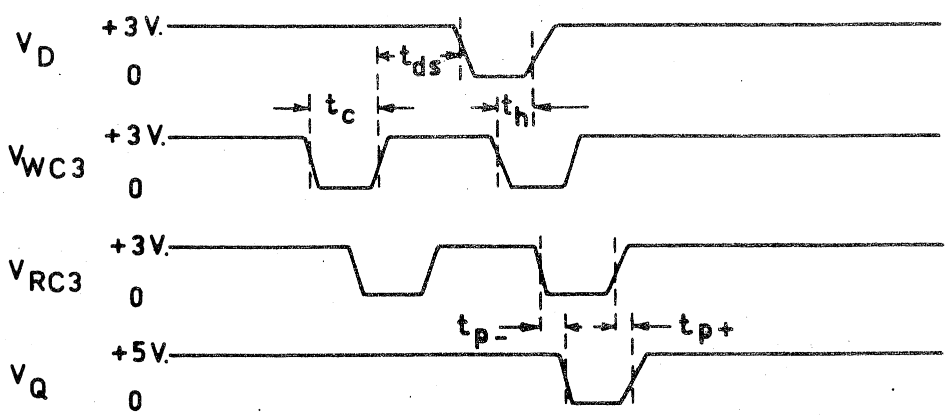


FIG. 4. TYPICAL SWITCHING WAVEFORMS.